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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,815	06/11/2001	Hassan S. Hashemi	00CON159PC-CIP1	3172

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,815	HASHEMI ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,29 and 31-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,29,31-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 10, 2004 has been entered.

Response to 37 C.F.R. 1.131 Affidavit

2. Upon further review and consideration of the Affidavit filed December 2, 2002, it has been determined that the Affidavit was insufficient to overcome the file date of Patent No. 6,377,464 to Hashemi et al. for the following reasons:

3. The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Hashemi reference to either a constructive reduction to practice or an actual reduction to practice. The entire period during which diligence is required must be accounted for. Applicant has merely stated that due diligence has been exercised in reducing the invention to practice, which falls short of the required showing of diligence. It has been held that stating that the subject matter "was diligently reduced to practice" is not a showing but a mere pleading (*In re Harry,* 333 F.2d 920, 923,142 USPQ 164, 166 (CCPA 1964)). A 2-day period lacking activity has been held to be fatal. *In re Mulder*, 716 F.2d 1542, 1545, 219 USPQ 189, 193 (Fed. Cir. 1983)(37 CFR 1.131 issue).

Furthermore, there is no showing of reasonable diligence of the attorney in preparing and filing the patent application on behalf of the inventive entity.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 27, 29 and 31 – 55 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,377,464 to Hashemi et al.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Hashemi el al. disclose a structure comprising:

a substrate (Figure 6 (608) having a top surface for receiving a die (Figure 6 (602);

a printed circuit board (see, for example, Col. 12, lines 9 - 12 and 29 - 32) attached to a bottom surface of said substrate;

a support pad (604) attached to the top surface of the substrate, said support pad being coupled to a ground bond pad (Col. 6, lines 44 – 48) of the die by a down bonding wire, said die being mounted on the support pad;

at least one via (Figure 6 (6O6a)) in said substrate; and

said at least one via providing an electrical connection between a signal bond pad (which is located on the chip at the chip end of signal wire (622) as illustrated in Figure 6) of said die and said printed circuit board (which is not illustrated but is taught, see above).

Regarding claims 2, 3, 4, and 5, Hashemi et al. disclose a structure, as recited above, further disclosing a semiconductor die (Figure 6 (602), an organic substrate (Col. 4, line 21), wherein the organic substrate is FR4 based laminate (Col. 4, lines 26 - 31, and a ceramic substrate (Col. 3, Lines 20 - 21).

Regarding claim 6, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 6, via that is under substrate bond pad (632)) provides an electrical connection between a substrate bond pad (632) and said printed circuit board (not shown, discussed above), wherein said substrate bond pad is electrically connected to said signal bond pad (at die end of wire (622) of said die.

Regarding claim 7, Hashemi el al. disclose a structure, as recited above, further disclosing:

wherein said at least one via (i.e., the via that is connected to signal bond pads in Figure 6) abuts said substrate bond pad (632).

Regarding claim 8, Hashemi el al. disclose a structure, as recited above, further disclosing wherein the substrate bond pad Figure 6 (632) is electrically connected to said signal bond pad of said die by a signal bonding wire (Figure 6 (622)).

Regarding claim 9, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) provides an electrical connection between said signal bond pad (denoted by 730) of said die (710) and a land (714), said land being electrically connected to said printed circuit board (not shown but discussed above).

Regarding claim 10: Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) abuts said land (714).

Regarding claim 11, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) provides an electrical connection between a substrate bond pad (pad on substrate, not specifically illustrated, but indicated as connection between substrate and wire (730)) and a land (714), wherein said substrate bond pad is electrically connected to said signal bond pad of said die (pad on die, not specifically illustrated, but indicated as connection between wire (730) and die (710)).

Regarding claim 12, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via bond pad (see above) and said land (714) (Figure 7 (708)) abuts said substrate.

Regarding claims 13 and 14, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said substrate bond pad is electrically connected to said signal bond pad of said die by a signal bonding wire (Figure 7 (730)).

regarding claims 15 and 16, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) comprises copper (Col.4. lines 31 - 32 in conjunction with Col. 5, lines 40 - 44 and Col. 6, lines 29 - 32).

Regarding claims 17 – 19, 27 and 29, Hashemi el al. disclose a structure comprising:

a substrate (Figure 6 (608) having a top surface for receiving a die (Figure 6 (602);

a printed circuit board (see, for example, Col. 12, lines 9 - 12 and 29 - 32) attached to a bottom surface of said substrate;

a support pad (604) attached to the top surface of the substrate, said support pad being coupled to a ground bond pad (Col. 6, lines 44 – 48) of the die by a down bonding wire, said die being mounted on the support pad;

at least one via (Figure 6) in said substrate; and

said at least one via providing an electrical connection between a signal bond pad (which is located on the chip at the chip end of signal wire (622) as illustrated in Figure 6) of said die and said printed circuit board (which is not illustrated but is taught, see above).

Further disclosing wherein a heat spreader is attached to bottom surface of substrate and said first via (see, for example, Figure 7 (708)) providing a connection between said semiconductor die and said heat spreader (see, for example, Col. 6, lines 10 – 30, note: Figure 6 illustrates an analogous arrangement) wherein said heat spreader is an electrical conductor (Col. 6, lines 19 – 20) and where said heat spreader is attached to a printed circuit board (Col. 7, lines 2 – 5).

Regarding claim 20, Hashemi el al. disclose a structure, as recited above, further comprising a substrate down bond area attached to said top surface of said substrate (Figure 7, downbonds (730)) connected to die attach pad (732), see also Col. 7, line 41 - 42).

Regarding claim 21, Hashemi et al. disclose a structure, as recited above, further disclosing wherein said first via (Figure 7 (708) provides an electrical connection between said substrate down bond area (732) and said heat spreader (that is connected to (714) (see above).

Regarding claim 22, Hashemi el a/. disclose a structure, as recited above, further disclosing wherein a semiconductor die (Figure 7 (710)) ground bond pad on said semiconductor die is electrically connected to said substrate down bond area) by a down bonding wire (730) (see also, Col. 7 lines 41 - 42).

Regarding claim 23, Hashemi et al. disclose a structure, wherein the heat spreader is attached by solder (Col. 6, lines 33 – 39).

Regarding claim 24, Hashemi et al. disclose a structure, wherein the heat spreader is a thermal conductor.

Regarding claim 25, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said heat spreader is attached to a printed circuit board by solder (see, for example, Col. 3, lines 17 - 21).

Regarding claim 26, Hashemi et al. disclose a structure, as recited above, further disclosing wherein a second via (Figure 6 (606) connected to bond pad (632)) provides an electrical connection (wires (622) between a signal bond pad of said semiconductor die (602) and a printed circuit board substrate down bond area (as discussed above).

Regarding claims 31 – 33, Hashemi et al. disclose a structure, as recited above, further disclosing a semiconductor die (Figure 6 (602), an organic substrate (Col. 4, line 21), wherein the organic substrate is FR4 based laminate (Col. 4, lines 26 – 31, and a ceramic substrate (Col. 3, lines 20 - 21).

Regarding claims 36 and 41, Hashemi et al. disclose a structure, wherein the substrate bond pad is electrically connected to the signal bond pad of the semiconductor die by a signal bonding wire.

Regarding claim 38, Hashemi el al. disclose a structure, wherein the second via abuts the land.

Regarding claims 34, 37, and 39, Hashemi el al. disclose a structure, as recited above, further disclosing wherein said second via (Figure 6 (606) as discussed above) provides an electrical connection (wires (622) or (620)) between a substrate bond pad (632) and a land (not illustrated in Figure 6 but taught in Col. 12, lines 18 - 24, and see Figure 5, lands (510)), wherein said substrate bond pad of said pad (Figure 6 (632) is

electrically connected to said signal semiconductor die (602) and wherein said land is electrically connected to said printed circuit board (as discussed above).

Regarding claims 35 and 40, Hashemi et al. disclose a structure, as recited above, further disclosing wherein said second via (Figure 6 (606) connected to substrate bond pad (632)) abuts said substrate bond pad (632) and said land (not illustrated in Figure 6 but taught in Col. 12, lines 18 - 24, and see Figure 5, lands (510), as discussed above).

Regarding claims 42 and 43, Hashemi et al. disclose a structure, wherein the first and second vias comprise copper.

Regarding claim 44, Hashemi el al. disclose a structure comprising:

Hashemi el al. disclose a structure comprising:

a substrate (Figure 6 (608) having a top surface for receiving a die (Figure 6 (602);

a printed circuit board (see, for example, Col. 12, lines 9 - 12 and 29 - 32) attached to a bottom surface of said substrate;

a support pad (604) attached to the top surface of the substrate, said support pad being coupled to a ground bond pad (Col. 6, lines 44 – 48) of the die by a down bonding wire, said die being mounted on the support pad;

a heat spreader is attached to bottom surface of substrate;

a plurality of vias (Figure 6) in said substrate; and

said plurality of vias providing a connection between said semiconductor die (602) and said heat spreader which is attached to ground conductive pads (610).

Regarding claim 45, Hashemi et al. disclose a structure, wherein the heat spreader is attached to a printed circuit board, as discussed above.

Regarding claim 46, Hashemi el al. disclose a structure, as recited above, further disclosing wherein a second plurality of vias (Figure 6, un-referenced vias (606)) providing a connection between a plurality of signal bond pads (not referenced but connected to wire (622)) of said semiconductor die (602) and said printed circuit board (as discussed above).

Regarding claim Hashemi et al. disclose a structure, further comprising a substrate down bond area attached to the top surface of the substrate.

Regarding claims 48 and 50, Hashemi et al. disclose a structure, wherein the first plurality of vias provide an electrical connection between the substrate down bond area and the heat spreader, as discussed above.

Regarding claim 49, Hashemi et al. disclose a structure, wherein a ground bond pad on the semiconductor die is electrically connected to the substrate down bond area by a down bonding wire, as discussed above.

Regarding claim 51, Hashemi et al. teach a structure, wherein the first plurality of vias provides a thermal connection between the semiconductor die and heat spreader, as discussed above.

Regarding claim 52, Hashemi et al. teach a structure, wherein the second plurality of vias provide electrical connections between a plurality of substrate bond pads and the printed circuit board, wherein each of the plurality of bond pads is electrically connected to a respective one of the plurality of signal bond pads of the die.

Regarding claim 53, Hashemi et al. disclose a structure, as recited above, further disclosing wherein said second plurality of vias (Figure 6, un-referenced vias (606)) provide electrical connections between each one of said plurality of signal bond pads of said semiconductor die (602) and a respective one of a plurality of lands (4610) as taught in Col. 12, lines 18 - 24 which teaches using a plurality of exposed attachment pads), said plurality of lands being electrically connected to said printed circuit board (as discussed above).

Regarding claims 54 and 55, Hashemi et al. disclose a structure, wherein the vias comprise copper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens
Patent Examiner